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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,899	12/16/2003	Atsuhiro Otaka	032172	5713

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
TRUONG, LOAN	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,899	OTAKA ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-26* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-6, and 8-26 are rejected under 35 U.S.C. 102(a) as being anticipated by Lin (US 2002/0099974).

In regard to claim 1, Lin disclosed a redundancy management method for BIOS, comprising the steps of:

using one of a pair of memories, which respectively store the BIOS for setting hardware in an environment in which OS can use said hardware, for operation and the other for standby (*Primary BIOS and Secondary BIOS, fig. 1A)*;

switching to the BIOS in said memory in standby when the BIOS in said one memory cannot be booted (*Confirmation signal not received, then shadow secondary BIOS, fig. 2)*; and

executing an update of said BIOS by writing to said memory in standby (*if verification code finds that secondary BIOS is corrupted it may cause secondary BIOS to be overwritten by a copy of the functional primary BIOS, fig. 1A, 404, 40s, paragraph 0050).*

In regard to claim 2, Lin disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of permitting switching said memory in standby to in operation when the update of said BIOS in said memory in standby succeeded (*select value 40b in the BIOS setup values 40v is check to indicates that the secondary BIOS program is to be used, fig. 1A, 40, paragraph 0043).*

In regard to claim 3, Lin disclosed the redundancy management method according to claim 2, further comprising a step of switching said permitted memory in standby to in operation, and said memory in operation to in standby when said hardware is started up (*set the GPIO2 register to a value that will place a value on the selection signal line indicates usage of the secondary BIOS program, fig. 3, 206, paragraph 0038).*

In regard to claim 4 Lin disclosed the redundancy management method for BIOS according to claim 3, further comprising a step of writing the BIOS of said memory switched to operation (*BIOS setup values, fig. 1A, 40v, paragraph 0031)* to said memory switched to standby for redundancy after said switching (*pure copying operation could be performed to place an identical copy of primary BIOS into the memory allocated for the secondary BIOS, fig. 1A, 40p, 40s, paragraph 0050).*

In regard to claim 5, Lin disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of preventing switching of said memory in standby to said memory in operation when the update of said BIOS in said memory in standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 6, Lin disclosed the redundancy management method for BIOS according to claim 4, further comprising a step of preventing switching said memory switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 8, Lin disclosed the redundancy management method for BIOS according to claim 4, further comprising a step of preventing execution of said redundancy step when said hardware is started up for power recovery (*secondary BIOS program may be overwritten by a copy of the functional primary BIOS in recovery operation, paragraph 0050).*

In regard to claim 9, Yang et al. disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of executing the update of BIOS in a memory in standby of another hardware connected with said hardware according to

the update of the BIOS in said memory in standby of said hardware (*recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS, paragraph 0050)*.

In regard to claim 10, Yang et al. disclosed the redundancy management method for BIOS according to claim 1, further comprising a step of executing the synchronization processing of the BIOS with another hardware connected with said hardware (*pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS, paragraph 0050)*.

In regard to claim 11, Yang et al. disclosed a data processing apparatus, comprising:

a hardware including a CPU (*fig. 1A, 20)*;

a pair of memories which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*primary BIOS and secondary BIOS, fig. 1A, 40p, 40s)*; and

a service processor for using one of said pair of memories for operation and the other for standby (*Primary BIOS and Secondary BIOS, fig. 1A)* when said hardware is started up and switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted (*Confirmation signal not received, then shadow secondary BIOS, fig. 2)*, wherein said CPU executes the update of said BIOS by writing to said memory in standby (*if verification code finds that secondary BIOS is corrupted it may cause secondary BIOS to be overwritten by a copy of the functional primary BIOS, fig.*

1A, 404, 40s, paragraph 0050).

In regard to claim 12, Lin disclosed the data processing apparatus according to claim 11, wherein said service processor permits switching said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded (*If the secondary BIOS program is present and has passed the checksum verification test then the GPIO2 register is set to indicate usage of the secondary BIOS program, fig. 3, 205, paragraph 0037).*

In regard to claim 13, Lin disclosed the data processing apparatus according to claim 12, wherein said service processor switches said permitted memory in standby to a memory in operation, and said memory in operation to said memory in standby when said hardware is started up (*primary BIOS has detected internal errors and BIOS switching circuit shadow in the secondary BIOS program, paragraph 0034).*

In regard to claim 14, Lin disclosed the data processing apparatus according to claim 13, wherein said CPU writes the BIOS of said memory switched to operation, to said memory switched to standby for redundancy after said switching (*secondary BIOS can provide verification code or attempt to correct corruption on the primary BIOS, paragraph 0050).*

In regard to claim 15, Lin disclosed the data processing apparatus according to claim 11, wherein said CPU prevents switching said memory in standby to the memory in

operation when the update of said BIOS in said memory in standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 16, Lin disclosed the data processing apparatus according to claim 14, wherein said CPU prevents switching said memory switched to standby, to said memory in operation when writing of said BIOS in said memory switched to standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 17, Lin disclosed the data processing apparatus according to claim 11, further comprising another hardware connected with said hardware, and said hardware executes the update of the BIOS in the memory in standby of said other hardware connected with said hardware according to the update of the BIOS in said memory in standby of said hardware (*recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS, paragraph 0050).*

In regard to claim 18, Lin disclosed the data processing apparatus according to claim 11, wherein said hardware executes the synchronization processing of the BIOS with said other hardware connected with said hardware (*pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS, paragraph 0050).*

In regard to claim 19, Lin disclosed a storage system, comprising: a storage control apparatus comprises:

a hardware including a CPU (*fig. 1A, 20)*;

a pair of memories which respectively store a BIOS for setting said hardware in an environment in which OS can use said hardware (*primary BIOS and secondary BIOS, fig. 1A, 40p, 40s)*; and

a service processor for using one of said pair of memories for operation and the other for standby (*Primary BIOS and Secondary BIOS, fig. 1A)* when said hardware is started up and switching to the BIOS in said memory in standby when the BIOS of said one memory cannot be booted (*Confirmation signal not received, then shadow secondary BIOS, fig. 2)*; and

a plurality of storage devices (*flash ROM to hold primary and secondary BIOS program, paragraph 0031)* connected to said storage control device (*primary and secondary BIOS programs are executed by the CPU, paragraph 0011)*, wherein said CPU of said storage control apparatus executes the update of said BIOS by writing to said memory in standby (*if verification code finds that secondary BIOS is corrupted it may cause secondary BIOS to be overwritten by a copy of the functional primary BIOS, fig. 1A, 404, 40s, paragraph 0050).*

In regard to claim 20, Lin disclosed the storage system according to claim 19, wherein said service processor of said storage control apparatus permits the switching of said memory in standby to said memory in operation when the update of said BIOS in said memory in standby succeeded (*If the secondary BIOS program is present and has*

passed the checksum verification test then the GPIO2 register is set to indicate usage of the secondary BIOS program, fig. 3, 205, paragraph 0037).

In regard to claim 21, Lin disclosed the storage system according to claim 20, wherein said service processor of said storage control apparatus switches said permitted memory in standby to a memory in operation (*If the primary BIOS program is corrupted, the computer system will automatically switch over to the secondary BIOS program, paragraph 0030)*, and said memory in operation to said memory in standby when said hardware is started up (*POST power-on-self-test allows primary BIOS program to test determine if it is functional, paragraph 0031).*

In regard to claim 22, Lin disclosed the storage system according to claim 21, wherein said CPU of said storage control apparatus writes the BIOS of said memory switched to operation, to said memory switched to standby for redundancy after said switching (*secondary BIOS can provide verification code or attempt to correct corruption on the primary BIOS, paragraph 0050).*

In regard to claim 23, Lin disclosed the storage system according to claim 19, wherein said CPU of said storage control apparatus prevents switching said memory in standby to the memory in operation when the update of said BIOS in said memory in standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 24, Lin disclosed the storage system according to claim 22, wherein said CPU of said storage control apparatus prevents switching said memory switched to standby, to said memory in operation, when writing of said BIOS in said memory switched to standby failed (*if secondary BIOS program has not passed the checksum verification test then primary BIOS program must continue to be used, fig. 3, 205, paragraph 0037).*

In regard to claim 25, Lin disclosed the storage system according to claim 19, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage control apparatus executes the update of the BIOS in the memory in standby of said other storage control apparatus according to the update of the BIOS in said memory in standby of said storage control apparatus (*recovery of BIOS by overwritten the secondary BIOS with a copy of the functional primary BIOS, paragraph 0050).*

In regard to claim 26, Lin disclosed the storage system according to claim 19, further comprising another storage control apparatus, which is connected to said storage devices and said storage control apparatus and for controlling said storage devices, wherein said storage control apparatus executes the synchronization processing of the BIOS with said other storage control apparatus (*pure copying operation performed to place an identical copy of the primary BIOS into secondary BIOS, paragraph 0050).*

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
AU 2114

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER